

LM5115 Secondary Side Post Regulator / Synchronous Buck Controller

General Description

The LM5115 is a versatile switching regulator controller. It has two main application configurations. The first is utilizing the Secondary Side Post Regulation (SSPR) technique to implement multiple output power converters. In the second configuration, it can be used as a standalone synchronous buck controller (Please see page 14 for more details). The SSPR technique develops a highly efficient and well regulated auxiliary output from the secondary side switching waveform of an isolated power converter. Regulation of the auxiliary output voltage is achieved by leading edge pulse width modulation (PWM) of the main channel duty cycle. Leading edge modulation is compatible with either current mode or voltage mode control of the main output. The LM5115 drives external high side and low side NMOS power switches configured as a synchronous buck regulator. A current sense amplifier provides overload protection and operates over a wide common mode input range. Additional features include a low dropout (LDO) bias regulator, error amplifier, precision reference, adaptive dead time control of the gate signals and thermal shutdown.

Features

- Self-synchronization to main channel output
- Standalone DC/DC Synchronous buck mode
- Leading edge pulse width modulation
- Voltage-mode control with current injection and input line feed-forward
- Operates from AC or DC input up to 75V
- Wide 4.5V to 30V bias supply range
- Wide 0.75V to 13.5V output range.
- Top and bottom gate drivers sink 2.5A peak
- Adaptive gate driver dead-time control
- Wide bandwidth error amplifier (4MHz)
- Programmable soft-start
- Thermal shutdown protection
- TSSOP-16 or thermally enhanced LLP-16 packages

Typical Application Circuit

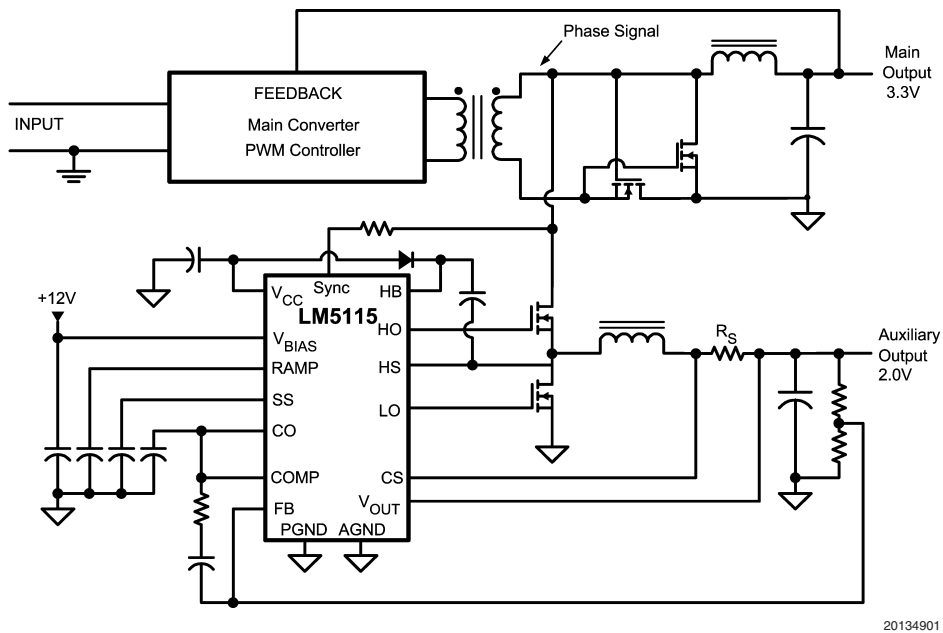
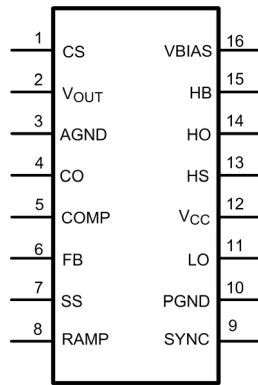


FIGURE 1. Simplified Multiple Output Power Converter Utilizing SSPR Technique

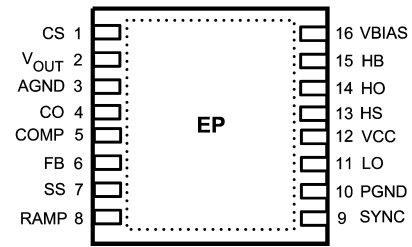
Connection Diagram



20134902

16-Lead TSSOP

See NS Package Numbers MTC16



20134921

16-Lead LLP

See NS Package Numbers SDA16A

Ordering Information

Ordering Number	Package Type	NSC Package Drawing	Supplied As
LM5115MTC	TSSOP-16	MTC16	92 Units Per Anti-Static Tube
LM5115MTCX	TSSOP-16	MTC16	2500 units shipped as Tape & Reel
LM5115SD	LLP-16	SDA16A	1000 units shipped as Tape & Reel
LM5115SDX	LLP-16	SDA16A	4500 units shipped as Tape & Reel

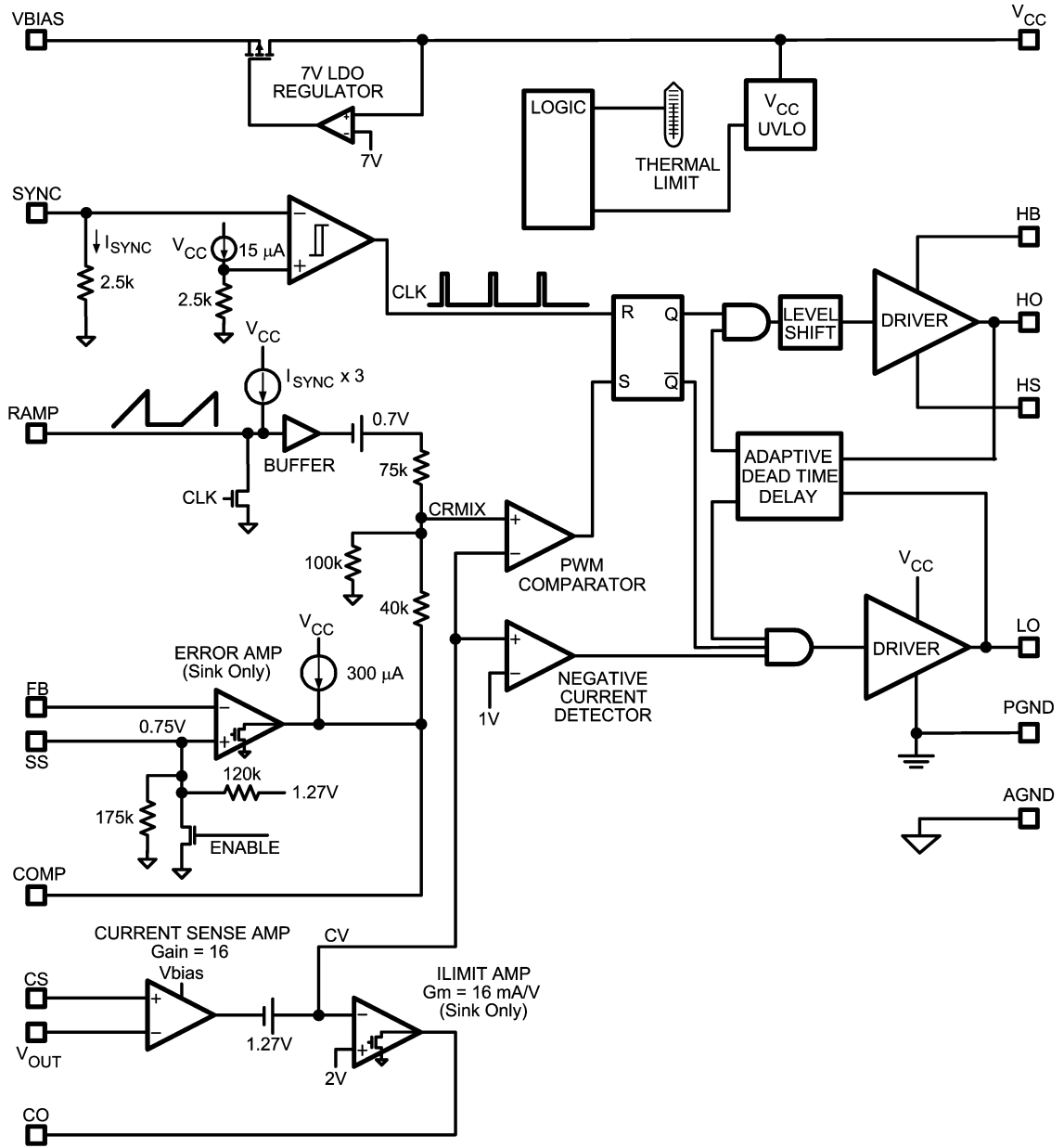
Pin Descriptions

Pin	Name	Description	Application Information
1	CS	Current Sense amplifier positive input	A low inductance current sense resistor is connected between CS and VOUT. Current limiting occurs when the differential voltage between CS and VOUT exceeds 45mV (typical).
2	VOUT	Current sense amplifier negative input	Connected directly to the output voltage. The current sense amplifier operates over a voltage range from 0V to 13.5V at the VOUT pin.
3	AGND	Analog ground	Connect directly to the power ground pin (PGND).
4	CO	Current limit output	For normal current limit operation, connect the CO pin to the COMP pin. Leave this pin open to disable the current limit function.
5	COMP	Compensation. Error amplifier output	COMP pin pull-up is provided by an internal 300uA current source.
6	FB	Feedback. Error amplifier inverting input	Connected to the regulated output through the feedback resistor divider and compensation components. The non-inverting input of the error amplifier is internally connected to the SS pin.
7	SS	Soft-start control	An external capacitor and the equivalent impedance of an internal resistor divider connected to the bandgap voltage reference set the soft-start time. The steady state operating voltage of the SS pin equal to 0.75V (typical).
8	RAMP	PWM Ramp signal	An external capacitor connected to this pin sets the ramp slope for the voltage mode PWM. The RAMP capacitor is charged with a current that is proportional to current into the SYNC pin. The capacitor is discharged at the end of every cycle by an internal MOSFET.
9	SYNC	Synchronization input	A low impedance current input pin. The current into this pin sets the RAMP capacitor charge current and the frequency of an internal oscillator that provides a clock for the free-run (DC input) mode .

Pin Descriptions (Continued)

Pin	Name	Description	Application Information
10	PGND	Power Ground	Connect directly to the analog ground pin (AGND).
11	LO	Low side gate driver output	Connect to the gate of the low side synchronous MOSFET through a short low inductance path.
12	VCC	Output of bias regulator	Nominal 7V output from the internal LDO bias regulator. Locally decouple to PGND using a low ESR/ESL capacitor located as close to controller as possible.
13	HS	High side MOSFET source connection	Connect to negative terminal of the bootstrap capacitor and the source terminal of the high side MOSFET.
14	HO	High side gate driver output	Connect to the gate of high side MOSFET through a short low inductance path.
15	HB	High side gate driver bootstrap rail	Connect to the cathode of the bootstrap diode and the positive terminal of the bootstrap capacitor. The bootstrap capacitor supplies current to charge the high side MOSFET gate and should be placed as close to controller as possible.
16	VBIAS	Supply Bias Input	Input to the LDO bias regulator and current sense amplifier that powers internal blocks. Input range of VBIAS is 4.5V to 30V.
-	Exposed Pad (LLP Package Only)	Exposed Pad, underside of LLP package	Internally bonded to the die substrate. Connect to system ground for low thermal impedance.

Block Diagram



20134903

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

VBIAS to GND	-0.3V to 32V
VCC to GND	-0.3V to 9V
HS to GND	-1V to 76V
VOUT, CS to GND	-0.3V to 15V
All other inputs to GND	-0.3V to 7.0V
Storage Temperature Range	-55°C to +150°C
Junction Temperature	+150°C

ESD Rating

HBM (Note 2)

2 kV

Operating Ratings

VBIAS supply voltage	5V to 30V
VCC supply voltage	5V to 7.5V
HS voltage	0V to 75V
HB voltage	VCC + HS
Operating Junction Temperature	-40°C to +125°C

Typical Operating Conditions

PARAMETER	MIN	TYP	MAX	UNITS
Supply Voltage, VBIAS	4.5		30	V
Supply Voltage, VCC	4.5		7	V
Supply voltage bypass, CVBIAS	0.1	1		μF
Reference bypass capacitor, CVCC	0.1	1	10	μF
HB-HS bootstrap capacitor	0.047			μF
SYNC Current Range (VCC = 4.5V)	50		150	μA
RAMP Saw Tooth Amplitude	1		1.75	V
VOUT regulation voltage (VBIAS min = 3V + VOUT)	0.75		13.5	V

Electrical Characteristics

Unless otherwise specified, $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$, VBIAS = 12V, No Load on LO or HO.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VBIAS SUPPLY						
Ibias	VBIAS Supply Current	$F_{\text{SYNC}} = 200\text{kHz}$			4	mA
VCC LOW DROPOUT BIAS REGULATOR						
VccReg	VCC Regulation	VCC open circuit. Outputs not switching	6.65	7	7.15	V
	VCC Current Limit	(Note 4)		40		mA
	VCC Under-voltage Lockout Voltage	Positive going VCC	4		4.5	V
	VCC Under-voltage Hysteresis		0.2	0.25	0.3	V
SOFT-START						
	SS Source Impedance		43	60	77	kΩ
	SS Discharge Impedance			100		Ω
ERROR AMPLIFIER and FEEDBACK REFERENCE						
VREF	FB Reference Voltage	Measured at FB pin	0.737	0.75	0.763	V
	FB Input Bias Current	FB = 2V		0.2	0.5	μA
	COMP Source Current			300		μA
	Open Loop Voltage Gain			60		dB
GBW	Gain Bandwidth Product			4		MHz
Vio	Input Offset Voltage		-7	0	7	mV
	COMP Offset	Threshold for $V_{\text{HO}} = \text{high RAMP} = \text{CS} = \text{VOUT} = 0\text{V}$		2		V
	RAMP Offset	Threshold for $V_{\text{HO}} = \text{high COMP} = 1.5\text{V}$, CS = VOUT = 0V		1.1		V
CURRENT SENSE AMPLIFIER						
	Current Sense Amplifier Gain			16		V/V
	Output DC Offset			1.27		V
	Amplifier Bandwidth			500		kHz

Electrical Characteristics

Unless otherwise specified, $T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{\text{BIAS}} = 12\text{V}$, No Load on LO or HO. (Continued)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CURRENT LIMIT						
	ILIMIT Amp Transconductance			16		mA / V
	Overall Transconductance			237		mA / V
	Positive Current Limit	$V_{\text{CL}} = V_{\text{CS}} - V_{\text{VOUT}}$ $V_{\text{OUT}} = 6\text{V}$ and $\text{CO/COMP} = 1.5\text{V}$	37	45	53	mV
	Positive Current Limit Foldback	$V_{\text{CL}} = V_{\text{CS}} - V_{\text{VOUT}}$ $V_{\text{OUT}} = 0\text{V}$ and $\text{CO/COMP} = 1.5\text{V}$	31	38	45	mV
VCLneg	Negative Current Limit	$V_{\text{OUT}} = 6\text{V}$ $V_{\text{CL}} = V_{\text{CS}} - V_{\text{VOUT}}$ to cause LO to shutoff		-17		mV
RAMP GENERATOR						
	SYNC Input Impedance			2.5		k Ω
	SYNC Threshold	End of cycle detection threshold		15		μA
	Free Run Mode Peak Threshold	RAMP peak voltage with dc current applied to SYNC.			2.3	V
	Current Mirror Gain	Ratio of RAMP charge current to SYNC input current.	2.7		3.3	A/A
	Discharge Impedance			100		Ω
LOW SIDE GATE DRIVER						
V_{OLL}	LO Low-state Output Voltage	$I_{\text{LO}} = 100\text{mA}$		0.2	0.5	V
V_{OHL}	LO High-state Output Voltage	$I_{\text{LO}} = -100\text{mA}$, $V_{\text{OHL}} = V_{\text{CC}} - V_{\text{LO}}$		0.4	0.8	V
	LO Rise Time	$C_{\text{LOAD}} = 1000\text{pF}$		15		ns
	LO Fall Time	$C_{\text{LOAD}} = 1000\text{pF}$		12		ns
I_{OHL}	Peak LO Source Current	$V_{\text{LO}} = 0\text{V}$		2		A
I_{OLL}	Peak LO Sink Current	$V_{\text{LO}} = 12\text{V}$		2.5		A
HIGH SIDE GATE DRIVER						
V_{OLH}	HO Low-state Output Voltage	$I_{\text{HO}} = 100\text{mA}$		0.2	0.5	V
V_{OHH}	HO High-state Output Voltage	$I_{\text{HO}} = -100\text{mA}$, $V_{\text{OHH}} = V_{\text{HB}} - V_{\text{HO}}$		0.4	0.8	V
	HO Rise Time	$C_{\text{LOAD}} = 1000\text{pF}$		15		ns
	HO High Side Fall Time	$C_{\text{LOAD}} = 1000\text{pF}$		12		ns
I_{OHH}	Peak HO Source Current	$V_{\text{HO}} = 0\text{V}$		2		A
I_{OLH}	Peak HO Sink Current	$V_{\text{HO}} = 12\text{V}$		2.5		A
SWITCHING CHARACTERISTICS						
	LO Fall to HO Rise Delay	$C_{\text{LOAD}} = 0$		70		ns
	HO Fall to LO Rise Delay	$C_{\text{LOAD}} = 0$		50		ns
	SYNC Fall to HO Fall Delay	$C_{\text{LOAD}} = 0$		120		ns
	SYNC Rise to LO Fall Delay	$C_{\text{LOAD}} = 0$		50		ns
THERMAL SHUTDOWN						
T_{SD}	Thermal Shutdown Temp.		150	165		$^{\circ}\text{C}$
	Thermal Shutdown Hysteresis			25		$^{\circ}\text{C}$
THERMAL RESISTANCE						
θ_{JA}	Junction to Ambient	MTC Package		125		$^{\circ}\text{C/W}$
θ_{JA}	Junction to Ambient	SDA Package		32		$^{\circ}\text{C/W}$

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

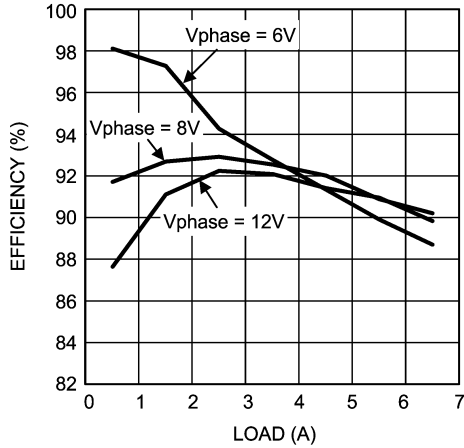
Note 2: The human body model is a 100 pF capacitor discharged through a 1.5k Ω resistor into each pin.

Note 3: Min and Max limits are 100% production tested at 25 $^{\circ}\text{C}$. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate National's Average Outgoing Quality Level (AOQL).

Note 4: Device thermal limitations may limit usable range.

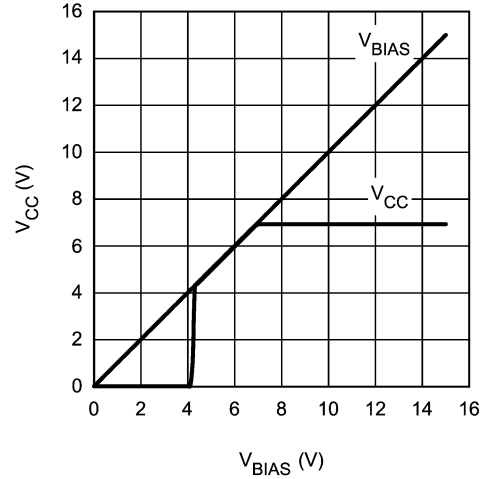
Typical Performance Characteristics

Efficiency vs. Load Current and V_{phase}



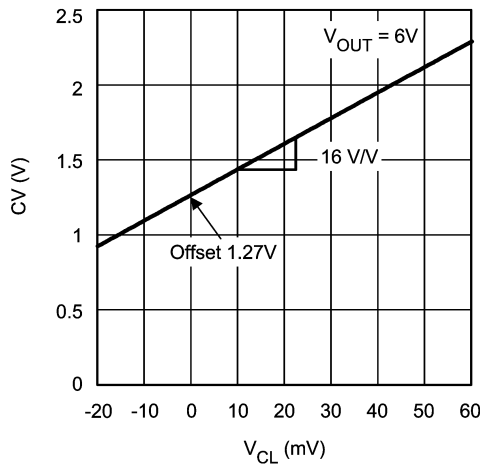
20134922

V_{CC} Regulator Start-up Characteristics, V_{CC} vs. V_{BIAS}



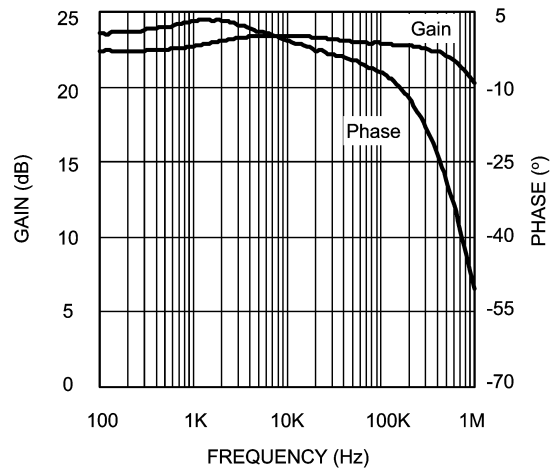
20134904

Current Value (CV) vs. Current Limit (V_{CL})



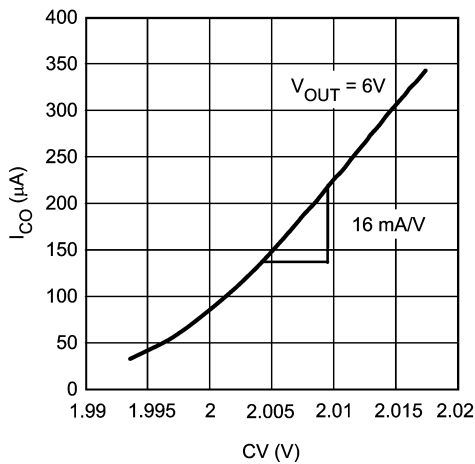
20134906

Current Sense Amplifier Gain and Phase vs. Frequency



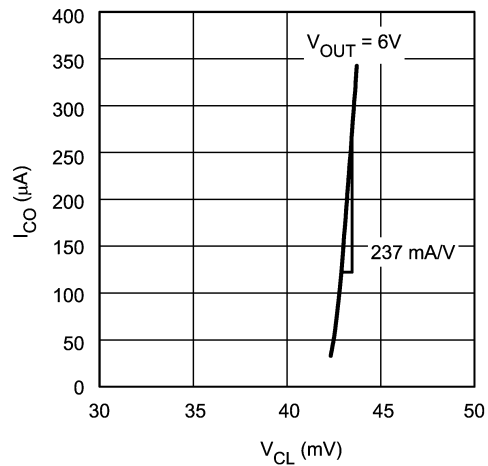
20134907

Current Error Amplifier Transconductance



20134908

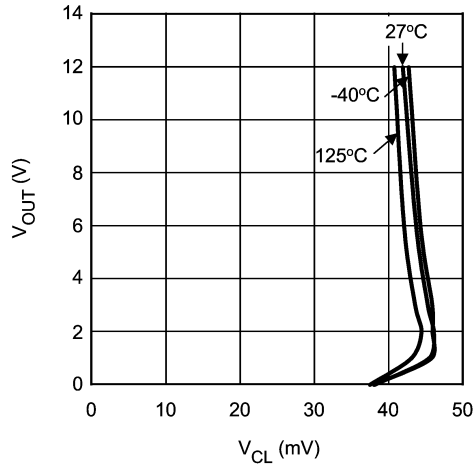
Overall Current Amplifier Transconductance



20134909

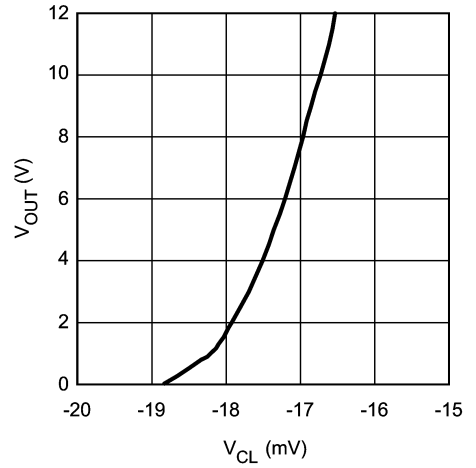
Typical Performance Characteristics (Continued)

Common Mode Output Voltage vs. Positive Current Limit



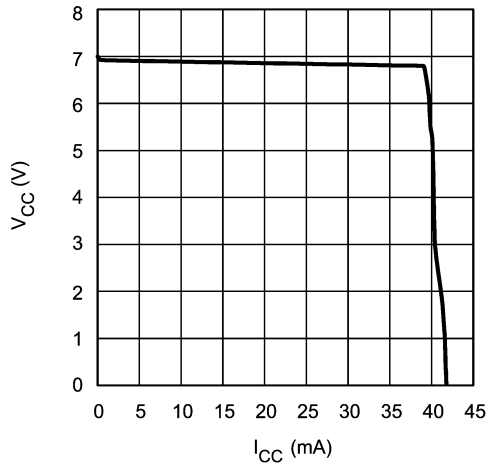
20134910

Common Mode Output Voltage vs. Negative Current Limit (Room Temp)



20134911

V_{CC} Load Regulation to Current Limit



20134905

Detailed Operating Description

The LM5115 controller contains all of the features necessary to implement multiple output power converters utilizing the Secondary Side Post Regulation (SSPR) technique. The SSPR technique develops a highly efficient and well regulated auxiliary output from the secondary side switching waveform of an isolated power converter. Regulation of the auxiliary output voltage is achieved by leading edge pulse width modulation (PWM) of the main channel duty cycle. Leading edge modulation is compatible with either current mode or voltage mode control of the main output. The LM5115 drives external high side and low side NMOS power switches configured as a synchronous buck regulator. A current sense amplifier provides overload protection and operates over a wide common mode input range from 0V to 13.5V. Additional features include a low dropout (LDO) bias regulator, error amplifier, precision reference, adaptive dead time control of the gate driver signals and thermal shutdown. A programmable oscillator provides a PWM clock signal when the LM5115 is powered by a dc input (free-run mode) instead of the phase signal of the main channel converter (SSPR mode).

Low Drop-Out Bias Regulator (VCC)

The LM5115 contains an internal LDO regulator that operates over an input supply range from 4.5V to 30V. The output of the regulator at the VCC pin is nominally regulated at 7V and is internally current limited to 40mA. VCC is the main supply to the internal logic, PWM controller, and gate driver circuits. When power is applied to the VBIAS pin, the regulator is enabled and sources current into an external capacitor connected to the VCC pin. The recommended output

capacitor range for the VCC regulator is 0.1 μ F to 100 μ F. When the voltage at the VCC pin reaches the VCC under-voltage lockout threshold of 4.25V, the controller is enabled. The controller is disabled if VCC falls below 4.0V (250mV hysteresis). In applications where an appropriate regulated dc bias supply is available, the LM5115 controller can be powered directly through the VCC pin instead of the VBIAS pin. In this configuration, it is recommended that the VCC and the VBIAS pins be connected together such that the external bias voltage is applied to both pins. The allowable VCC range when biased from an external supply is 4.5V to 7V.

Synchronization (SYNC) and Feed-Forward (RAMP)

The pulsing "phase signal" from the main converter synchronizes the PWM ramp and gate drive outputs of the LM5115. The phase signal is the square wave output from the transformer secondary winding before rectification (*Figure 1*). A resistor connected from the phase signal to the low impedance SYNC pin produces a square wave current (I_{SYNC}) as shown in *Figure 2*. A current comparator at the SYNC input monitors I_{SYNC} relative to an internal 15 μ A reference. When I_{SYNC} exceeds 15 μ A, the internal clock signal (CLK) is reset and the capacitor connected to the RAMP begins to charge. The current source that charges the RAMP capacitor is equal to 3 times the I_{SYNC} current. The falling edge of the phase signal sets the CLK signal and discharges the RAMP capacitor until the next rising edge of the phase signal. The RAMP capacitor is discharged to ground by a low impedance (100 Ω) n-channel MOSFET. The input impedance at SYNC pin is 2.5k Ω which is normally much less than the external SYNC pin resistance.

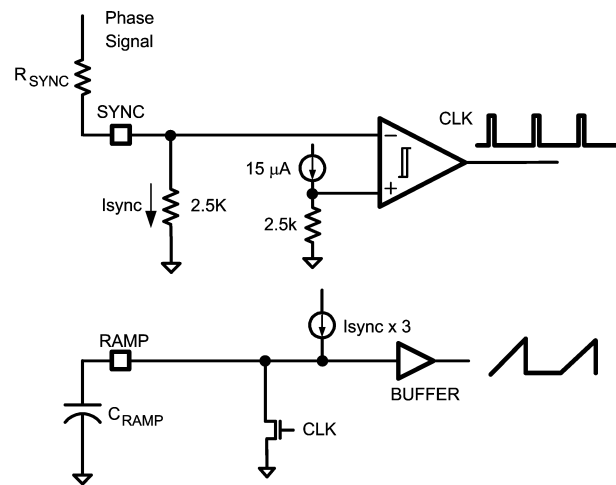


FIGURE 2. Line Feed-Forward Diagram

The RAMP and SYNC functions illustrated in *Figure 2* provide line voltage feed-forward to improve the regulation of the auxiliary output when the input voltage of the main converter changes. Varying the input voltage to the main converter produces proportional variations in amplitude of the phase signal. The main channel PWM controller adjusts the pulse width of the phase signal to maintain constant volt*seconds and a regulated main output as shown in *Fig-*

ure 3. The variation of the phase signal amplitude and duration are reflected in the slope and duty cycle of the RAMP signal of the LM5115 ($I_{SYNC} \propto$ phase signal amplitude). As a result, the duty cycle of the LM5115 is automatically adjusted to regulate the auxiliary output voltage with virtually no change in the PWM threshold voltage. Transient line regu-

Synchronization (SYNC) and Feed-Forward (RAMP) (Continued)

lation is improved because the PWM duty cycle of the auxiliary converter is immediately corrected, independent of the delays of the voltage regulation loop.

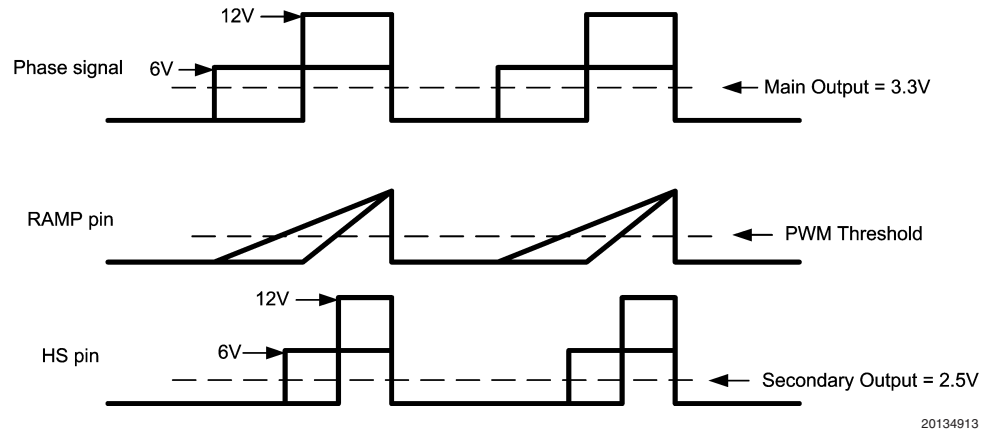


FIGURE 3. Line Feed-forward Waveforms

The recommended SYNC input current range is 50 μ A to 150 μ A. The SYNC pin resistor (R_{SYNC}) should be selected to set the SYNC current (I_{SYNC}) to 150 μ A with the maximum phase signal amplitude, $V_{PHASE(max)}$. This will guarantee that I_{SYNC} stays within the recommended range over a 3:1 change in phase signal amplitude. The SYNC pin resistor is therefore:

$$R_{SYNC} = (V_{PHASE(max)} / 150\mu A) - 2.5k\Omega$$

Once I_{SYNC} has been established by selecting R_{SYNC} , the RAMP signal amplitude may be programmed by selecting the proper RAMP pin capacitor value. The recommended peak amplitude of the RAMP waveform is 1V to 1.75V. The C_{RAMP} capacitor is chosen to provide the desired RAMP amplitude with the nominal phase signal voltage and pulse width.

$$C_{RAMP} = (3 \times I_{SYNC} \times T_{ON}) / V_{RAMP}$$

Where

C_{RAMP} = RAMP pin capacitance

I_{SYNC} = SYNC pin current

T_{ON} = corresponding phase signal pulse width

V_{RAMP} = desired RAMP amplitude (1V to 1.75V)

For example,

Main channel output = 3.3V. Phase signal maximum amplitude = 12V. Phase signal frequency = 250kHz

- Set $I_{SYNC} = 150\mu A$ with phase signal at maximum amplitude (12V):

$$I_{SYNC} = 150\mu A = V_{PHASE(max)} / (R_{SYNC} + 2.5 k\Omega) = 12V / (R_{SYNC} + 2.5 k\Omega)$$

$$R_{SYNC} = 12V/150\mu A - 2.5k\Omega = 77.5k\Omega$$

- $T_{ON} = \text{Main channel duty cycle} / \text{Phase frequency} = (3.3V/12V) / 250kHz = 1.1\mu s$
- Assume desired $V_{RAMP} = 1.5V$
- $C_{RAMP} = (3 \times I_{SYNC} \times T_{ON}) / V_{RAMP} = (3 \times 150\mu A \times 1.1\mu s) / 1.5V$
- $C_{RAMP} = 330pF$

Error Amplifier and Soft-Start (FB, CO, & COMP, SS)

An internal wide bandwidth error amplifier is provided within the LM5115 for voltage feedback to the PWM controller. The amplifier's inverting input is connected to the FB pin. The output of the auxiliary converter is regulated by connecting a voltage setting resistor divider between the output and the FB pin. Loop compensation networks are connected between the FB pin and the error amplifier output (COMP). The amplifier's non-inverting input is internally connected to the SS pin. The SS pin is biased at 0.75V by a resistor divider connected to the internal 1.27V bandgap reference. When the VCC voltage is below the UVLO threshold, the SS pin is discharged to ground. When VCC rises and exceeds the positive going UVLO threshold (4.25V), the SS pin is released and allowed to rise. If an external capacitor is connected to the SS pin, it will be charged by the internal resistor divider to gradually increase the non-inverting input of the error amplifier to 0.75V. The equivalent impedance of the SS resistor divider is nominally 60k Ω which determines the charging time constant of the SS capacitor. During start-up, the output of the LM5115 converter will follow the exponential equation:

$$VOUT(t) = VOUT(final) \times (1 - \exp(-t/R_{SS} \times C_{SS}))$$

Where

R_{SS} = internal resistance of SS pin (60k Ω)

C_{SS} = external Soft-Start capacitor

$VOUT(final)$ = regulator output set point

The initial $\Delta v / \Delta t$ of the output voltage is $VOUT(final) / R_{SS} \times C_{SS}$ and $VOUT$ will be within 1% of the final regulation level after 4.6 time constants or when $t = 4.6 \times R_{SS} \times C_{SS}$.

Pull-up current for the error amplifier output is provided by an internal 300 μ A current source. The PWM threshold signal at the COMP pin can be controlled by either the open drain error amplifier or the open drain current amplifier connected through the CO pin to COMP. Since the internal error ampli-

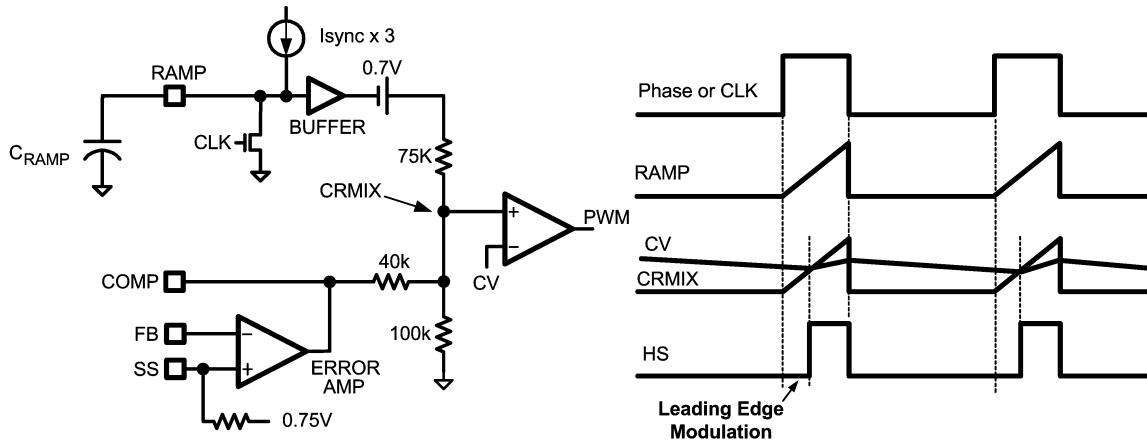
Error Amplifier and Soft-Start (FB, CO, & COMP, SS) (Continued)

fier is configured as an open drain output it can be disabled by connecting FB to ground. The current sense amplifier and current limiting function will be described in a later section.

Leading Edge Pulse Width Modulation

Unlike conventional voltage mode controllers, the LM5115 implements leading edge pulse width modulation. A current source equal to 3 times the I_{SYNC} current is used to charge

the capacitor connected to the RAMP pin as shown in *Figure 4*. The ramp signal and the output of the error amplifier (COMP) are combined through a resistor network to produce a voltage ramp with variable dc offset (CRMIX in *Figure 4*). The high side MOSFET which drives the HS pin is held in the off state at the beginning of the phase signal. When the voltage of CRMIX exceeds the internal threshold voltage CV, the PWM comparator turns on the high side MOSFET. The HS pin rises and the MOSFET delivers current from the main converter phase signal to the output of the auxiliary regulator. The PWM cycle ends when the phase signal falls and power is no longer supplied to the drain of the high side MOSFET.

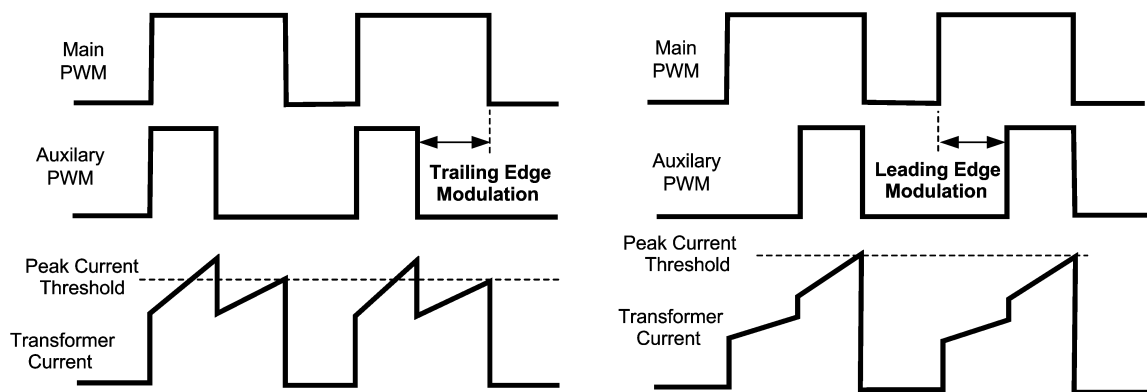


20134914

FIGURE 4. Synchronization and Leading Edge Modulation

Leading edge modulation of the auxiliary PWM controller is required if the main converter is implemented with peak current mode control. If trailing edge modulation were used, the additional load on the transformer secondary from the auxiliary channel would be drawn only during the first portion of the phase signal pulse. Referring to *Figure 5*, the turn off the high side MOSFET of the auxiliary regulator would create a non-monotonic negative step in the transformer cur-

rent. This negative current step would produce instability in a peak current mode controller. With leading edge modulation, the additional load presented by the auxiliary regulator on the transformer secondary will be present during the latter portion of the phase signal. This positive step in the phase signal current can be accommodated by a peak current mode controller without instability.



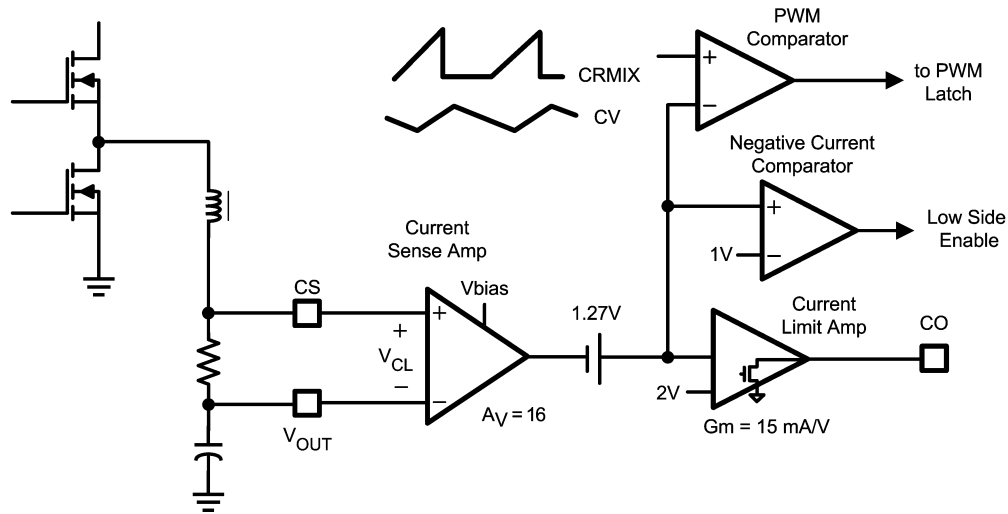
20134920

FIGURE 5. Leading versus Trailing Edge Modulation

Voltage Mode Control with Current Injection

The LM5115 controller uniquely combines elements and benefits of current mode control in a voltage mode PWM controller. The current sense amplifier shown in *Figure 6* monitors the inductor current as it flows through a sense resistor connected between CS and VOUT. The voltage gain

of the sense amplifier is nominally equal to 16. The current sense output signal is shifted by 1.27V to produce the internal CV reference signal. The CV signal is applied to the negative input of the PWM comparator and compared to CRMIX as illustrated in *Figure 4*. Thus the PWM threshold of the voltage mode controller (CV) varies with the instantaneous inductor current. Insure that the Vbias voltage is at least 3V above the regulated output voltage (VOUT).



20134915

FIGURE 6. Current Sensing and Limiting

Injecting a signal proportional to the instantaneous inductor current into a voltage mode controller improves the control loop stability and bandwidth. This current injection eliminates the lead R-C lead network in the feedback path that is normally required with voltage mode control (see *Figure 7*). Eliminating the lead network not only simplifies the compensation, but also reduces sensitivity to output noise that could pass through the lead network to the error amplifier.

The design of the voltage feedback path through the error amp begins with the selection of R1 and R2 in *Figure 7* to set the regulated output voltage. The steady state output voltage after soft-start is determined by the following equation:

$$V_{OUT}(\text{final}) = 0.75V \times (1 + R1/R2)$$

The parallel impedance of the R1, R2 resistor divider should be approximately 2k Ω (between 0.5k Ω and 5k Ω). Lower resistance values may not be properly driven by the error

amplifier output and higher feedback resistances can introduce noise sensitivity. The next step in the design process is selection of R3, which sets the ac gain of the error amplifier. The ac gain is given by the following equation and should be set to a value less than 30.

$$\text{GAIN}(\text{ac}) = R3/(R1 \parallel R2) < 30$$

The capacitor C1 is connected in series with R3 to increase the dc gain of the voltage regulation loop and improve output voltage accuracy. The corner frequency set by R3 x C1 should be less than 1/10th of the cross-over frequency of the overall converter such that capacitor C1 does not add phase lag at the crossover frequency. Capacitor C2 is added to reduce the noise in the voltage control loop. The value of C2 should be less than 500pF and C2 may not be necessary with very careful PC board layout.

Gate Drivers Outputs (HO & LO)

(Continued)

side MOSFET. The high side pulse is terminated when the phase signal falls and SYNC input comparator resets the PWM latch.

Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event the maximum junction temperature limit is exceeded. When activated, typically at 165 degrees Celsius, the controller is forced into a low power standby state with the output drivers and the bias regulator disabled. The device will restart when the junction temperature falls below the thermal shutdown hysteresis, which is typically 25 degrees. The thermal protection feature is provided to prevent catastrophic failures from accidental device overheating.

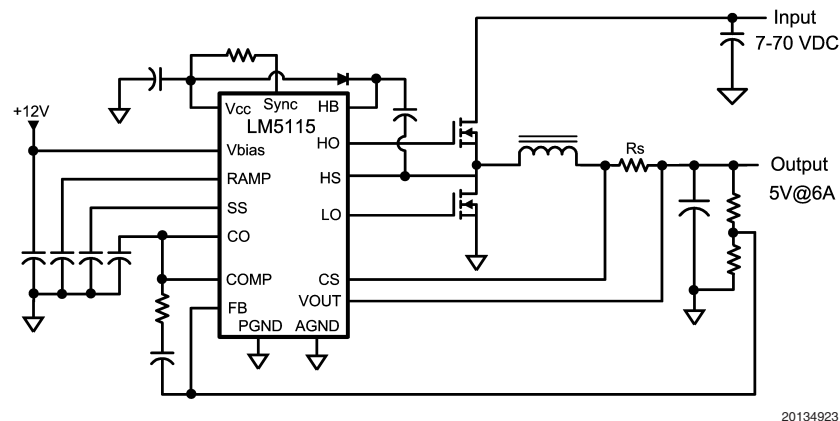
Standalone DC/DC Synchronous Buck Mode

The LM5115 can be configured as a standalone DC/DC synchronous buck controller. In this mode the LM5115 uses

leading edge modulation in conjunction with valley current mode control to control the synchronous buck power stage. The internal oscillator within the LM5115 sets the clock frequency for the high and low side drivers of the external synchronous buck power MOSFETs. The clock frequency in the synchronous buck mode is programmed by the SYNC pin resistor and RAMP pin capacitor. Connecting a resistor between a dc bias supply and the SYNC pin produces a current, I_{SYNC} , which sets the charging current of the RAMP pin capacitor. The RAMP capacitor is charged until its voltage reaches the peak ramp threshold of 2.25V. The RAMP capacitor is then discharged for 300ns before beginning a new PWM cycle. The 300ns reset time of the RAMP pin sets the minimum off time of the PWM controller in this mode. The internal clock frequency in the synchronous buck mode is set by I_{SYNC} , the ramp capacitor, the peak ramp threshold, and the 300ns deadtime.

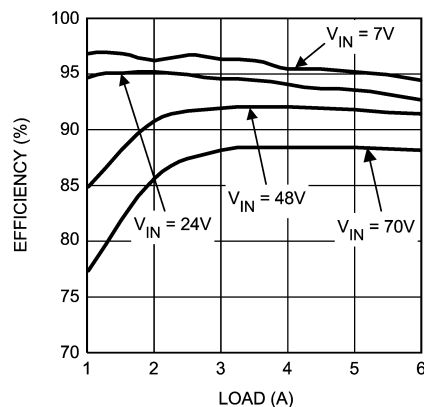
$$F_{CLK} \cong 1 / ((C_{RAMP} \times 2.25V) / (I_{SYNC} \times 3) + 300ns)$$

See the LM5115 dc evaluation board (AN-1367) for more details on the synchronous buck mode.



20134923

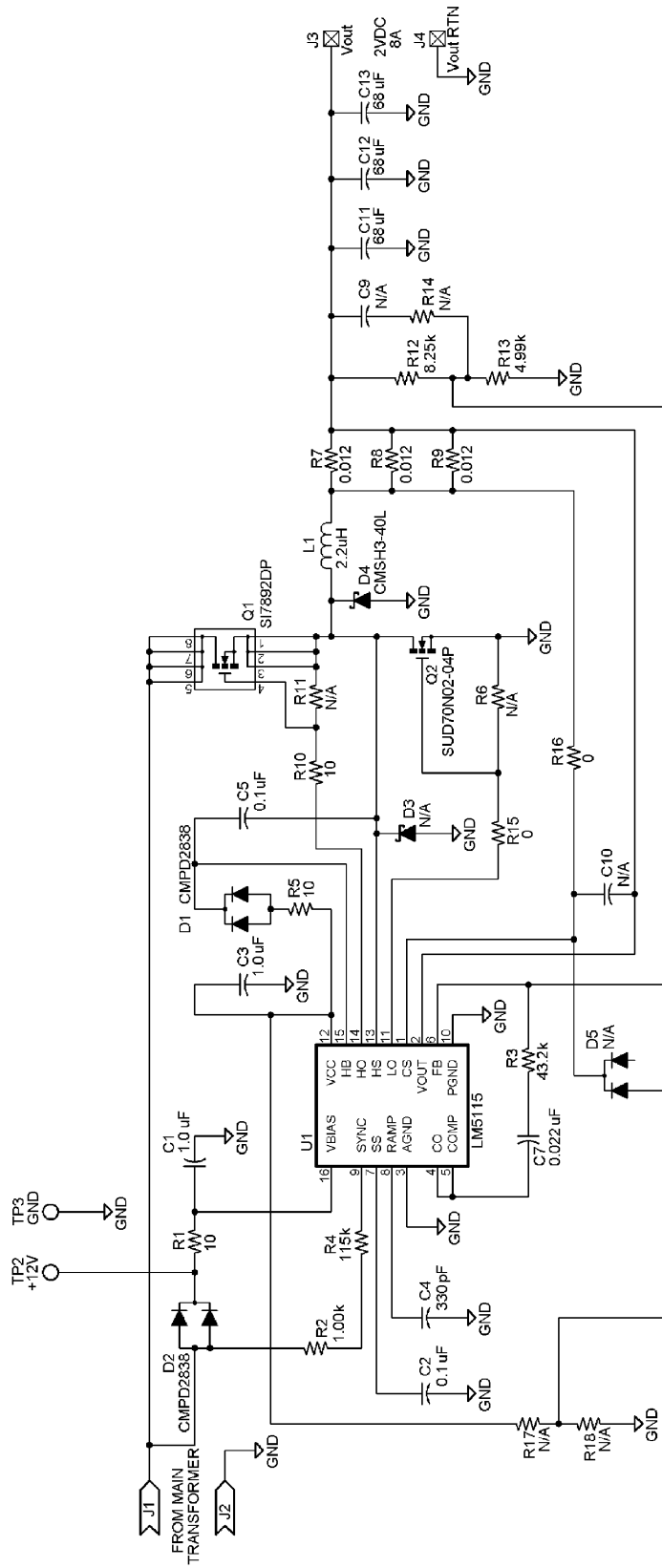
FIGURE 8. Simplified Typical Application Circuit (Synchronous Buck Mode)



20134924

FIGURE 9. Efficiency vs. Load Current and V_{IN} (Synchronous Buck Mode)

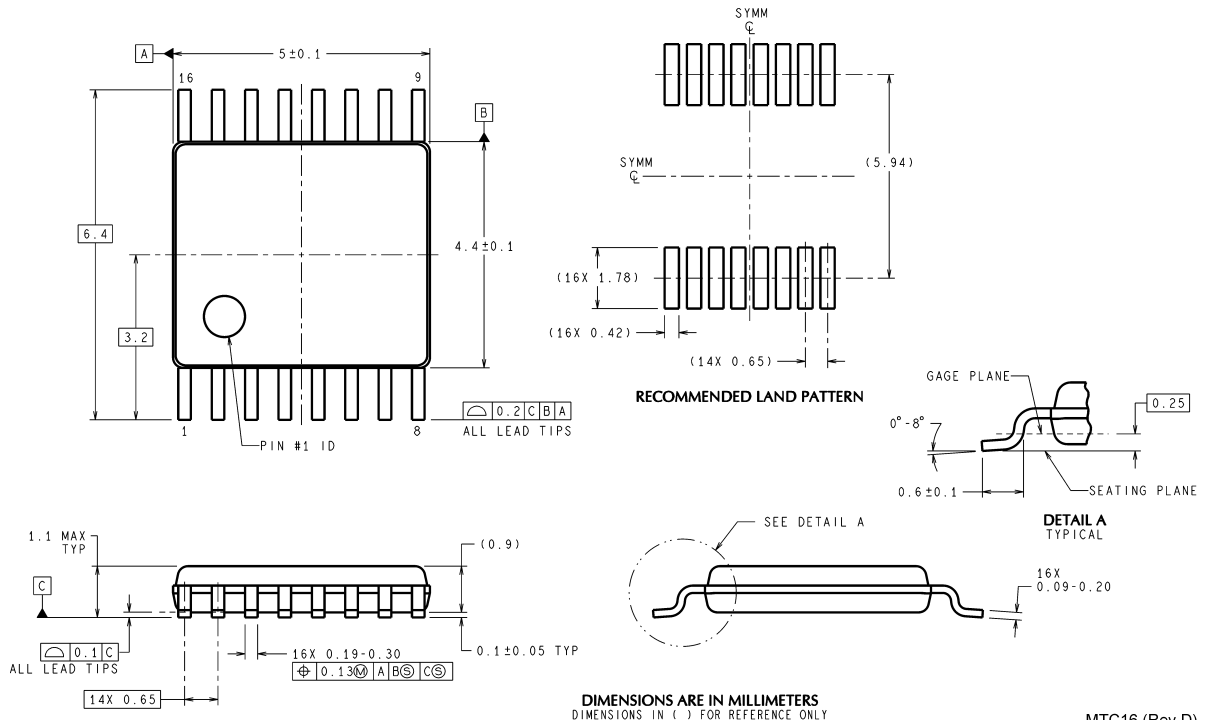
Application Circuit



20134917

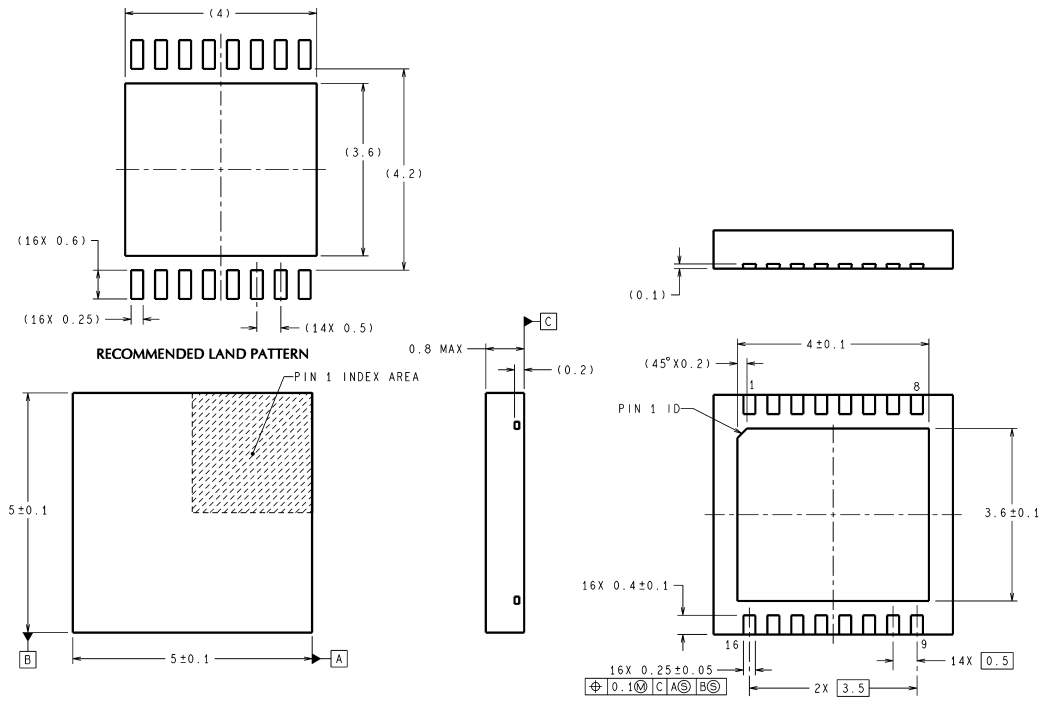
LM5115 Secondary Side Post Regulator
 (Inputs from LM5025 Forward Active Clamp Converter, 36V to 78V)

Physical Dimensions inches (millimeters) unless otherwise noted



MTC16 (Rev D)

TSSOP-16 Outline Drawing
NS Package Number MTC16



SDA16A (Rev A)

LLP-16 Outline Drawing
NS Package Number SDA16A

Notes

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.
 For the most current product information visit us at www.national.com.

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

- | | |
|--|---|
| <p>1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.</p> | <p>2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.</p> |
|--|---|

BANNED SUBSTANCE COMPLIANCE

National Semiconductor follows the provisions of the Product Stewardship Guide for Customers (CSP-9-111C2) and Banned Substances and Materials of Interest Specification (CSP-9-111S2) for regulatory environmental compliance. Details may be found at: www.national.com/quality/green.

Lead free products are RoHS compliant.



National Semiconductor
Americas Customer
Support Center
 Email: new.feedback@nsc.com
 Tel: 1-800-272-9959

National Semiconductor
Europe Customer Support Center
 Fax: +49 (0) 180-530 85 86
 Email: europe.support@nsc.com
 Deutsch Tel: +49 (0) 69 9508 6208
 English Tel: +44 (0) 870 24 0 2171
 Français Tel: +33 (0) 1 41 91 8790

National Semiconductor
Asia Pacific Customer
Support Center
 Email: ap.support@nsc.com

National Semiconductor
Japan Customer Support Center
 Fax: 81-3-5639-7507
 Email: jpn.feedback@nsc.com
 Tel: 81-3-5639-7560